modifications may be made to such embodiments without departing from the teachings of the present invention. For example, it is apparent that other types of memory cell elements beyond those illustrated in the foregoing detailed description can be formed using the teachings of the present invention. Accordingly, it is intended that the all such alterations and modifications be included within the scope and spirit of the invention as defined by the following claims.

What is claimed is:

1. A hybrid multi-bit magnetoelectronic memory device comprising:

a plurality of separate magnetic spin based memory elements situated on a semiconductor substrate;

wherein each magnetic spin based memory element stores a bit of data in the form of an electron spin state associated with a ferromagnetic layer, so that a plurality of data bits can be stored in said magnetic memory elements in the form of a plurality of separate electron spin states;

further wherein said magnetic spin based memory elements are arranged in a stack on the semiconductor substrate and configured so that all of said separate electron spin states can be read out at the same time.

2. The hybrid multi-bit memory device of claim 1, wherein each magnetic spin based memory element is a three terminal magnetic spin transistor.

3. The hybrid multi-bit memory device of claim 1, further including a semiconductor isolation element coupled to said plurality of separate magnetic spin based memory elements.

4. The hybrid multi-bit memory device of claim 1, wherein said semiconductor isolation element is a field effect transistor.

5. The hybrid multi-bit memory device of claim 1, wherein an entire byte worth of data can be read at once from said stack arrangement of magnetic spin based memory elements.

6. The hybrid multi-bit memory device of claim 1, wherein each magnetic spin based memory element is formed in a separate layer.

7. A hybrid multi-layer magnetoelectronic memory device comprising:

a plurality of separate magnetic spin based memory elements situated within a plurality of separate corresponding storage layers on a semiconductor substrate;

wherein each magnetic spin based memory element stores a bit of data in the form of an electron spin state associated with a ferromagnetic layer, so that a plurality of data bits can be stored in said magnetic memory elements in the form of a plurality of separate electron spin states;

a plurality of separate insulating layers interposed between said separate corresponding storage layers for insulating said separate magnetic spin based memory elements from each other.

8. The hybrid multi-layer memory device of claim 7, wherein each magnetic spin based memory element is a three terminal magnetic spin transistor.

9. The hybrid multi-layer memory device of claim 7, further including a first semiconductor isolation element coupled to said plurality of separate magnetic spin based memory elements.

10. The hybrid multi-layer memory device of claim 7, wherein said semiconductor isolation element is a field effect transistor.

11. The hybrid multi-layer memory device of claim 7, further including a plurality of thin film semiconductor isolation elements situated in layers between said plurality of magnetic spin based memory elements.

12. The hybrid multi-bit memory cell of claim 7, wherein each magnetic spin based memory element is formed in a separate layer.

13. A hybrid multi-layer magnetoelectronic memory device comprising:

a plurality of separate magnetic spin based memory elements situated within a stack arrangement of a plurality of separate corresponding storage layers on a semiconductor substrate;

a plurality of separate insulating layers interposed between said separate corresponding storage layers for insulating said separate magnetic spin based memory elements;

wherein each magnetic spin based memory element stores a bit of data in the form of an electron spin state associated with a ferromagnetic layer, so that a plurality of data bits can be stored in said magnetic memory elements in the form of a plurality of separate electron spin states;

further wherein each magnetic spin based memory element includes a unique transimpedance compared to other magnetic spin based memory elements in said stack arrangement.

14. The hybrid multi-layer magnetoelectronic memory device of claim 13, wherein multiple data bits can be read out at the same time by deconvolving an output voltage of the magnetoelectronic memory device to determine a value of individual bits for each magnetic spin based memory element.

15. The hybrid multi-layer magnetoelectronic memory device of claim 13, wherein each of said plurality of magnetic spin based memory elements includes a magnetic spin transistor with an associated ferromagnetic collector, ferromagnetic emitter, and base.

16. The hybrid multi-layer magnetoelectronic memory device of claim 13, further including a semiconductor isolation element used to isolate an output of such device.

17. The hybrid multi-layer magnetoelectronic memory device of claim 16, wherein said semiconductor isolation element is a field effect transistor.

18. The hybrid multi-layer magnetoelectronic memory device of claim 17, wherein said field effect transistor is situated in said semiconductor substrate.

19. The hybrid multi-layer magnetoelectronic memory device of claim 17, wherein said field effect transistor is situated in a thin film layer.

20. The hybrid multi-layer magnetoelectronic memory device of claim 13, wherein said unique transimpedance is set by configuring a base material associated with each of said magnetic spin based memory elements.